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Term	Documents
(17 AND 5).USPT,JPAB,EPAB,DWPI,TDBD.	117
(L17 AND L5).USPT,JPAB,EPAB,DWPI,TDBD.	117

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L18

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Search History

DATE: Friday, April 05, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ			
L18	L17 and l5	117	L18
L17	l13 same (protect or protecting or protection)	531	L17
L16	(protect or protection) and l15	124	L16
L15	l13 same l5	341	L15
L14	l13 and l5	1727	L14
L13	(identifier or bit or flag or register) same (indicate or specify or indicating or specifing) same (block or area or space) same (erase or erased or erasing or overwrite or overwriting or program or reprogram or programming or reprogramming or write or writing)	13144	L13
DB=USPT; PLUR=YES; OP=ADJ			
L12	5592641.pn.	1	L12
L11	5603056.pn.	1	L11
L10	5721877.pn.	1	L10
L9	6009495.pn.	1	L9
DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ			
L8	5930826[uref]	2	L8
L7	(prevent or preventing) same (unintentional) same (erase or erasing or overwrite or overwriting or reprogram or reprogramming) same l5	8	L7
L6	(flag same boot same (area or block)) and l5	89	L6
L5	nonvolatile memory or ((non adj volatile) adj memory) EEPROM or flash	170454	L5
L4	(unlock or unlocking) same parity same release	2	L4
L3	reserve same (lock or locking) same parity	1	L3
L2	L1	55	L2
DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ			
L1	((lock or locking) same parity) and RAID	60	L1

END OF SEARCH HISTORY

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L3: Entry 47 of 163 File: USPT Jul 18, 2000

DOCUMENT-IDENTIFIER: US 6091658 A
TITLE: Nonvolatile memory implementation for electronic devices

Detailed Description Text (11):
One method for determining which memory location should receive the data involves associating an index bit to each memory area. As each memory area is written to, the index bit associated with the memory area is incremented. In this way, all the controller needs to do is determine if the index bit of the second memory location 28 is greater than the index bit of the third memory location 30 to determine which memory location will receive the data. By incrementing the index register for a given EEPROM area immediately after the data string is written ensures that partial or incomplete write operations are not misinterpreted as valid data strings.

L3: Entry 48 of 163 File: USPT Apr 25, 2000

DOCUMENT-IDENTIFIER: US 6055188 A
TITLE: Nonvolatile semiconductor memory device having a data circuit for erasing and writing operations

CLAIMS:

9. A nonvolatile semiconductor memory device according to claim 8, wherein a number of said memory cell groups is n (n is a natural number equal to or larger than 2), the data includes the first to the m-th (m is a natural number equal to or larger than 2 and equal to or smaller than n) data, said data circuit sets a potential of said node to a value indicating that the erasing or writing is completed when all of first to m-th data indicate that the erasing or writing of the memory cells are sufficient during erase or write verify read and sets a potential of said node to a value indicating that the erasing or writing is incomplete when at least one of the first to m-th data indicates that the erasing or writing of a memory cell is insufficient.

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L3: Entry 34 of 163 File: USPT Dec 3, 2002

DOCUMENT-IDENTIFIER: US 6490663 B1
TITLE: Electronic control apparatus having rewritable nonvolatile memory

Brief Summary Text (8):
If the control program has not been written into the rewritable nonvolatile memory or has been written incompletely only partly in the electronic control apparatus for some reason, such an incomplete operation occurs that the control object can not be controlled normally even when the electronic control apparatus executes the control program. This problem may be countered by providing data, which indicate whether the control program is written, in a specified address in the rewritable nonvolatile memory, and waiting for a rewriting request in a boot program (starting program) stored in the rewritable nonvolatile memory along with the control program when it is determined with the data that the control program has not been written.

L3: Entry 52 of 163 File: USPT Dec 7, 1999

DOCUMENT-IDENTIFIER: US 6000004 A
TITLE: Nonvolatile semiconductor memory device with write protect data settings for disabling erase from and write into a block, and erase and re-erase settings for enabling write into and erase from a block

Detailed Description Text (28):
As described above, in the flash memory of the present example, if the erase operation of the block 1 has ended abnormally, the EC data is not written into the EC data storage region 1b of the block 1. That is to say, if there is any possibility that the erase of the data within the block 1 is incomplete because of such an abnormal end of the erase operation, then the EC data is not written into the EC data storage region 1b of the block 1. Thus, the re-erase of the block 1 can be performed with certainty irrespective of the states of a WP signal and the BP data storage region 1a, and it is no longer necessary to issue a WP release command for switching the WP signal. In addition, by defining the BP data and the EC data as data of two bits or more, e.g., "10" or "100", even when the abnormal end of an erase operation occurs, there is no possibility that the data stored in the BP data storage region 1a and the EC data storage region 1b happen to respectively coincide with the BP data and the EC data. Consequently, such an abnormal end can be detected with certainty.